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Methods of Forming Capacitor Structures, and Capacitor Structures

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Methods of Forming Capacitor Structures, and Capacitor Structures

TECHNICAL FIELD

The invention pertains to methods of forming capacitor structures, and also pertains to capacitor structures.

BACKGROUND OF THE INVENTION

As silicon device sizes becoming increasingly smaller, and as a minimum feature size of CMOS devices approaches and goes below the 0.1 micrometer regime, very thin gate insulators can be required to keep the capacitance of a dynamic random access (DRAM) capacitor cell in a 30 femptofarad (fF) range. For instance, if insulators are formed of silicon dioxide, it can be necessary to keep the insulators to a thickness of less than 2 nanometers (20Å), and possibly even as thin as 1 nanometer (10Å). Further, even if the insulating material is kept to a suitable thickness, it can be required to form a very high aspect ratio, or very tall polysilicon capacitor structure, to achieve a desired capacitance in the range of 30 fF.

A commonly-used dielectric material is silicon dioxide (SiO_2). However, thin layers of silicon dioxide can have high leakage current density due to direct band-to-band tunneling current or Fowler-Nordheim tunneling current. Accordingly, high-k (dielectric constant) films such as TiO_2, Ta_2O_5, and Al_2O_3 have received interest as being possible

substitutions for silicon dioxide as dielectric materials in DRAM capacitors. The higher dielectric constants of high-k materials can allow the use of thicker insulators, which can have orders of magnitude less tunneling current than a thin insulator while still yielding the same capacitance value as the thin insulator.

A difficulty with the utilization of high dielectric constant insulating materials is that the materials can have poor interface characteristics with silicon, and a high density of interface states. Such interface states can cause poor reliability of a capacitor structure, in that they can charge with time under use conditions. The resulting electric fields can cause breakdown of the thin dielectric insulators.

Among the materials which may have application as substitute dielectric materials for DRAM capacitors are aluminum oxide, aluminum nitride, and aluminum oxynitride. Such materials can be referred to herein as AlO, AlN and AlON, respectively, with it being understood that the compounds are described in terms of chemical constituents rather than stoichiometry. Accordingly, even though aluminum oxide can be described herein as being AlO, the material would typically be in the form of Al_2O_3, and the designation AlO used herein indicates that the material comprises chemical constituents of aluminum and oxygen, rather than indicating a particular stoichiometry of such constituents.

Several pertinent physical characteristics of AlO, AlN and AlON are as follows. First, aluminum oxide is a direct band gap insulator

with a band gap of 7.6eV and a dielectric constant of from about 9 to about 12, depending upon whether the material is amorphous or crystalline. If the material is crystalline, the crystallographic orientation can also affect the dielectric constant. Aluminum nitride has a band gap of 6.2eV, and amorphous aluminum nitride has a dielectric constant of from about 6 to about 9.6.

Work performed with AlN gate insulators indicates that AlN can be used as a gate insulator in MIS C-V structures on GaAs and silicon. Further, it has been shown that the deposited AlN films can be oxidized to form an aluminum oxide layer. Such oxidation can fill pin holes in the gate insulator to avoid shorted device structures, in a similar way that SiON insulators can be utilized in conventional DRAM capacitor cells.

Aluminum nitride films can be grown epitaxially on silicon utilizing metal organic chemical vapor deposition (MOCVD). Alternatively, aluminum nitride films can be deposited by RF magnetron sputtering. Regardless of how the aluminum nitride films are formed, they can subsequently be oxidized by, for example, exposing the films to oxygen at a temperature of from about 800°C to about 1,000°C for a time of from about one hour to about four hours. The aluminum nitride films can be oxidized either partially or fully into Al_2O_3, depending on the initial thickness of the films, the oxidation temperature, and the time of exposure to the oxidation temperature.

The above-described methods for deposition of aluminum nitride would typically be considered to be high temperature methods, and would utilize temperatures of 1000°C or greater. Processes have also been developed for deposition of aluminum nitride films which utilize temperatures of less than 1000°C. Such processes comprise nitrogen implantation into aluminum films, and can, for example, utilize ion beams of nitrogen having beam energies in the range of 200 eV to 6 keV, and current densities up to 50 $\mu A/cm^2$. Such densities can be produced by a Penning source type ion gun with a magnetic lens. Also, aluminum nitride can be formed by MOCVD, or by electron cyclotron resonance (ECR) dual-ion-beam sputtering, as well as by ion-beam assisted deposition (IBAD) using a nitrogen ion beam energy of 0.1 keV, 0.2 keV, or 1.5 keV. Still other methods for deposition of aluminum nitride films include low-voltage ion plating with reactive DC-magnetron sputtering, and reactive sputtering.

Aluminum oxynitride can also be deposited by processes utilizing temperatures of less than 1000°C. For instance, aluminum oxynitride can be chemical vapor deposited utilizing $AlCl_3$, CO_2 and NH_3 as reactive gases in a nitrogen carrier, with the films grown from the mixed gases at a temperature of, for example, from 770°C to 900°C. Further, aluminum oxynitride films can be grown by electron cyclotron resonance plasma-assisted chemical vapor deposition.

Studies indicate that thin films of aluminum nitride, aluminum oxynitride, and aluminum oxide can be deposited by evaporation of aluminum nitride and simultaneous bombardment with one or both of nitrogen and oxygen. Also, aluminum nitride and aluminum oxynitride films have been prepared by ion assisted deposition, in which aluminum was electron-beam evaporated on a substrate with simultaneous nitrogen ion bombardment. Aluminum oxynitride films can also be formed by planar magnetron sputtering from an alumina target in a mixture of nitrogen and oxygen, and can be formed by reactive RF sputtering in a mixture of N_2 and O_2. Also, aluminum oxynitride diffusion barriers have been formed in a temperature range of from about 400°C to about 725°C by annealing silver/aluminum bi-layers on silicon dioxide substrates in an ammonia ambient.

Finally, aluminum nitride can be formed by plasma nitridation of metallic aluminum. The aluminum nitride can then be converted to aluminum oxide, or aluminum oxynitride, by exposure of the aluminum nitride to an oxygen plasma.

Aluminum nitride films have previously been grown on aluminum films by RF sputter etching the metallic aluminum films in an ammonia-rare gas plasma at temperatures near room temperature under relatively modest applied plasma voltages. The technique has been used to form oxide tunnel barriers on superconducting metals for Josephson devices. The process essentially uses the plasma to generate reactive ions which

then interact with a metallic surface to form an oxide film. Electric fields and ionic charges can be present which can control and accelerate ion migration across a developing oxide film, with the thickness of the oxide film increasing as a logarithm of reaction time. A steady, slow rate of physical sputtering can be maintained by utilizing bombardment with inert gas ions such that the growing oxide plateaus in thickness. The particular thickness can depend on the oxide properties and the plasma conditions. The plateau value can be reached by using parametric values to grow a given thickness, and/or by growing the thickness to a value greater than a desired thickness and then subsequently restoring parameters which reduce the thickness to the desired thickness. The oxide films formed by such procedures can be exceptionally uniform in thickness and other properties.

It is possible to extend RF sputter etching techniques to formation of aluminum nitride at temperatures of less than 200°C by utilizing an ammonia reacting gas rather than diatomic nitrogen (N_2). The ammonia can yield charged ions, while diatomic nitrogen produces neutrals whose diffusion through nitride is unaided by the field across the nitride. The concentration of charged ions produced in plasmas containing ammonia gas can be much smaller than the concentration of charged oxygen ions produced in an oxygen-containing plasma. Accordingly, it can be desired to preclude oxygen from a nitridation plasma if it is desired to avoid forming dielectric films comprised predominantly of oxygen anions. On

the other hand, if it is desired to form a film comprising aluminum oxynitride, it will be desired to introduce oxygen in addition to the nitrogen. One method of introducing oxygen in a low dose is to introduce the oxygen in the form of N_2O.

SUMMARY OF THE INVENTION

In one aspect, the invention encompasses a method of forming a capacitor structure. A first electrical node is formed, and a layer of metallic aluminum is formed over the first electrical node. Subsequently, an entirety of the metallic aluminum within the layer is transformed into one or more of AlN, AlON, and AlO, with the transformed layer being a dielectric material over the first electrical node. A second electrical node is then formed over the dielectric material. The first electrical node, second electrical node and dielectric material together define at least a portion of the capacitor structure.

In another aspect, the invention encompasses a capacitor structure which includes a first electrical node, a second electrical node, and a dielectric material between the first and second electrical nodes. The dielectric material consists essentially of aluminum, oxygen and nitrogen.

BRIEF DESCRIPTION OF THE DRAWINGS

Preferred embodiments of the invention are described below with reference to the following accompanying drawings.

Fig. 1 is a diagrammatic, cross-sectional view of a semiconductor wafer fragment at a preliminary processing step of a method of the present invention.

Fig. 2 is a view of the Fig. 1 wafer fragment shown at a processing step subsequent to that of Fig. 1.

Fig. 3 is a view of the Fig. 1 wafer fragment shown at a processing step subsequent to that of Fig. 2.

Fig. 4 is a view of the Fig. 1 wafer fragment shown at a processing step subsequent to that of Fig. 3.

Fig. 5 is a view of the Fig. 1 wafer fragment shown at a processing step subsequent to that of Fig. 2, and shown in accordance with a second embodiment method of the present invention.

Fig. 6 is a view of the Fig. 1 wafer fragment shown at a processing step subsequent to that of Fig. 5 in accordance with the second embodiment method of the present invention.

Fig. 7 is a diagrammatic, cross-sectional view of a semiconductor wafer fragment at a preliminary processing step of a third embodiment method of the present invention, and shown with numbering identical to that utilized in describing the embodiment of Figs. 1-4.

Fig. 8 is a view of the Fig. 7 wafer fragment shown at a processing step subsequent to that of Fig. 7 in accordance with the third embodiment method of the present invention.

Fig. 9 is a view of the Fig. 7 wafer fragment shown at a processing step subsequent to that of Fig. 7 in accordance with a fourth embodiment method of the present invention.

Fig. 10 is a view of the Fig. 1 wafer fragment shown at a processing step subsequent to that of Fig. 1, and shown in accordance with a fifth embodiment method of the present invention..

Fig. 11 is a view of the Fig. 1 wafer fragment shown at a processing step subsequent to that of Fig. 10 in accordance with the fifth embodiment method of the present invention.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

This disclosure of the invention is submitted in furtherance of the constitutional purposes of the U.S. Patent Laws "to promote the progress of science and useful arts" (Article 1, Section 8).

The invention encompasses new processes for forming capacitor structures wherein low-temperature processing is utilized to form one or more of aluminum nitride, aluminum oxynitride, or aluminum oxide within a dielectric material between two capacitor plates. The low temperature processing comprises forming a metallic layer of aluminum, and subsequently converting the metallic layer to one or more of aluminum nitride, aluminum oxynitride, or aluminum oxide. For purposes of interpreting this disclosure and the claims that follow, "low

temperature" processing is to be understood as processing occurring at less than or equal to 200°C.

Low temperature processing can provide numerous advantages for formation of semiconductor device structures. For instance, studies indicate that there is a tendency for fixed charges and fast states to develop on or within a few angstroms of an aluminum nitride/silicon interface, which can introduce some instabilities in the MIS electrical characteristics and long-term stabilities. At least some of the slow and fast states are attributable to the use of excessively high aluminum nitride deposition temperatures, characteristic of, for example, CVD processes. Such temperatures can allow for intermixing of components at the interface, doping of the silicon with aluminum, and even some formation of aluminum silicides. Forming aluminum nitride temperatures under 300°C may serve to mitigate this problem, in that the diffusion co-efficient of aluminum in silicon is roughly 10^{-24} cm^2sec^{-1}. Accordingly, aluminum penetration into silicon at temperatures of about 300°C or below for exposure times of about 10,000 seconds will amount to only a small fraction of an angstrom diffusion distance. Further, penetration can be orders of magnitude less at temperatures of around 100°C to about 200°C. Accordingly, it can be possible to avoid autodoping; and maintain a clean, sharp interface if aluminum nitride, aluminum oxynitride and/or aluminum oxide can be formed at temperatures of less

than or equal to 200°C. Further, if plasmas can be avoided, it can be possible to avoid driving ions from a plasma into a silicon substrate.

An exemplary method of the present invention is described with reference to Figs. 1-4. Referring initially to Fig. 1, a semiconductor wafer fragment 10 is illustrated at a preliminary processing step of a method of the present invention. Semiconductor wafer fragment 10 comprises a substrate 12 which can comprise, for example, monocrystalline silicon lightly-doped with a background p-type dopant. To aid in interpretation of the claims that follow, the terms "semiconductive substrate" and "semiconductor substrate" are defined to mean any construction comprising semiconductive material, including, but not limited to, bulk semiconductive materials such as a semiconductive wafer (either alone or in assemblies comprising other materials thereon), and semiconductive material layers (either alone or in assemblies comprising other materials). The term "substrate" refers to any supporting structure, including, but not limited to, the semiconductive substrates described above.

A transistor gate 14 is shown formed over substrate 12. Gate 14 comprises a pad oxide layer 16, a conductively doped silicon layer 18, a silicide layer 20, and an insulative material 22. Pad oxide 16 can comprise, for example, silicon dioxide; silicon layer 18 can comprise, for example, polycrystalline silicon conductively doped with either an n-type or p-type dopant; silicide 20 can comprise, for example, tungsten silicide

or titanium silicide; and insulative material 22 can comprise, for example, silicon nitride or silicon dioxide.

Sidewall spacers 24 are shown formed along sidewalls of gate 14, and can comprise, for example, silicon dioxide or silicon nitride. Conductively-doped regions 26 and 28 are shown provided within substrate 12 and adjacent transistor gate 14. Conductively-doped regions 26 can be lightly doped and can correspond to, for example, lightly doped diffusion regions; while regions 28 can be more heavily doped, and can correspond to heavily doped source/drain regions. Regions 26 and 28 can be conductively doped with either n-type or p-type dopant. Gate 14 and doped regions 26 and 28 together define a transistor structure 30.

An isolation region 29 is adjacent one of the source/drain regions 28. Isolation region 29 can comprise, for example, silicon dioxide, and can correspond to a shallow trench isolation region.

An insulative material 32 is shown formed over substrate 12 and transistor structure 30. Insulative material 32 can comprise, for example, borophosphosilicate glass (BPSG). Further, insulative structure 32 can comprise multiple insulative materials, such as, for example, an underlying layer of chemical vapor deposited silicon dioxide and an upper layer of BPSG, even though layer 32 is illustrated in Fig. 1 as being a single material layer.

An opening has been formed through insulative material layer 32 to one of the source/drain regions 28, and subsequently filled with a conductive material 34. Conductive material 34 can comprise, for example, a metal and/or a conductively doped silicon. In particular embodiments, conductive material 34 comprises conductively-doped polycrystalline silicon. The polycrystalline silicon can be conductively-doped with either n-type or p-type dopant. Conductively material 34 ultimately comprises a first electrical node of a capacitor structure. Although conductive material 34 is shown with a planar upper surface, it is to be understood that conductive material 34 can have a roughened surface, such as, for example, a surface of hemispherical grain polysilicon. Also, although conductive material 34 is shown as a plug, it is to be understood that conductive material 34 can have other shapes, such as, for example, a container shape.

A metallic aluminum layer 36 is shown formed over conductive material 34. Metallic aluminum layer 36 can be formed by, for example, ion-assisted deposition of aluminum. Layer 36 preferably has a thickness of from greater than 0Å to about 40Å and can, for example, comprise a thickness of from about 5Å to about 15Å. The thickness of aluminum layer 36 can be controlled to within about 1Å. Residual surface oxides (not shown) can be removed from over an upper surface of conductive material 34 prior to formation of metallic aluminum material 36 utilizing, for example, a low-voltage sputter etching treatment.

Layer 36 is shown patterned to be provided only over conductive material 34, and not over insulative material 32. Such patterning can be accomplished by, for example, selective deposition of material 36 only over conductive material 34, or by patterning layer 36 after non-selective deposition. The patterning of non-selectively deposited material 36 can be accomplished by, for example, forming a patterned photoresist block (not shown) over a portion of material 36 that is on conductive material 34, while leaving other portions of material 36 not covered by the photoresist block, and subsequently etching the uncovered portions of material 36. The photoresist block can then be removed to leave the structure shown in Fig. 1.

Referring next to Fig. 2, wafer fragment 10 is shown after metallic aluminum layer 36 (Fig. 1) is exposed to conditions which convert the metallic aluminum to a dielectric material 40. Such conditions can convert layer 36 to one or more aluminum oxide, aluminum oxynitride, or aluminum nitride. Preferably, the conditions will comprise low-temperature transformation of material 36, with low-temperature being defined as a temperature less than or equal to 200°C. Utilization of low-temperature transformation can avoid exposure of the doped regions 26 and 28, or other doped regions associated with substrate 10, to excessive temperatures which could cause undesired diffusion of dopant from the doped regions to adjacent regions.

A thickness of dielectric material 40 can be determined from a starting thickness of metallic aluminum layer 36 (Fig. 1) as well as by the type of dielectric material ultimately formed. For instance, if the dielectric material is aluminum nitride, then a starting thickness of metallic aluminum layer 36 of about 20Å will yield a thickness of dielectric material 40 of from about 28.5Å to about 31.5Å, assuming that the metallic aluminum is entirely reacted. The metallic aluminum of layer 36 can be converted to dielectric material 40 by one or more of the methods described in the "Background" section of this disclosure, including, for example, exposing layer 36 to reactive RF sputtering in an ammonia/N_2O mixture; reactive RF sputtering of the aluminum in a N_2/O_2 mixture; reactive RF sputtering of the aluminum in a O_2 or a CO_2 environment to form aluminum oxide; nitrogen implantation into the metallic aluminum to form aluminum nitride; and electron cyclotron resonance plasma-assisted chemical vapor deposition utilizing N_2O/N_2. An exemplary process can utilize RF nitridation to form aluminum nitride from the metallic aluminum. Specifically, a substrate can be maintained at a temperature of about 25°C and can be exposed to plasma for a time of from about 10 minutes to about 20 minutes. A feed gas to the plasma can comprise at least 90% ammonia (by volume) and the remainder argon. The plasma can have a dynamic plasma pressure of about 10^{-2} torr, and can be maintained with a potential to an RF cathode plate of from about 300 volts to about 400 volts.

In the shown embodiment, an entirety of metallic aluminum of layer 36 (Fig. 1) is converted to dielectric material 40. Such dielectric material can consist essentially of, or consist of, aluminum nitride (AlN), aluminum oxynitride (AlON), or aluminum oxide (AlO) (with the listed compounds being described in terms of chemical constituents rather than stoichiometry). The dielectric material 40 can comprise a thickness of, for example, from greater than 0Å to less than 40Å, such as, for example, a thickness of from 5Å to 15Å, or a thickness of from 20Å to 40Å, or a thickness of from 10Å to 20Å. The desired thickness can depend on the dielectric constant of the dielectric material 40, and on a desired capacitance of a capacitor structure ultimately formed to comprise dielectric material 40. For instance, it can be desired that the thickness of aluminum oxynitride or aluminum nitride be from 10Å to 20Å for a DRAM capacitor having capacitance in a 30fF range. The relative dielectric constants of various materials are such that a layer of AlN can be twice as thick as a layer of SiO_2 and have about the same capacitance. Also, a layer of AlON can be twice as thick as a layer of SiO_2 and have about the same capacitance. Further, a material comprising a layer of AlON on a layer of AlN can be twice as thick as a layer of SiO_2 and have about the same capacitance. Additionally, a material comprising a layer of AlN on a layer of SiO_2 can be one and one-half times as thick as a material consisting of SiO_2 and have about the same capacitance.

Referring to Fig. 3, a conductive material 42 is formed over dielectric material 40. Conductive material 42 can comprise, for example, conductively doped silicon, and/or a metal. In the shown embodiment, conductive material 42 is illustrated as being patterned to have sidewalls coextensive with sidewalls of dielectric material 40. Such can be accomplished by, for example, forming conductive material 42 to extend past sidewalls of dielectric material 40, and then subsequently patterning conductive material 42 with photoresist (not shown) and an appropriate etch of conductive material 42. In alternative embodiments (not shown), conductive material 42 can be formed to extend beyond sidewalls of dielectric material 40 to define a capacitor plate which extends across several capacitor structures. Conductive material 42 defines a second electrical node which is spaced from first electrical node 34 by dielectric material 40. Accordingly, conductive material 42 is capacitively coupled with conductive material 34 through dielectric material 40; and materials 34, 40 and 42 together define a capacitor structure 44. Dielectric material 40 can be considered to define a dielectric region operatively positioned between electrical nodes 34 and 42 in the capacitor construction 44 of Fig. 4.

Referring next to Fig. 4, a conductive interconnection 50 is formed to extend through insulative material 32 and to a source/drain region 28 associated with transistor device 30. Interconnect 50 can comprise a bit line interconnect, and accordingly can be connected to a bit line 52.

Accordingly, transistor 30 and capacitor 44 can comprise a DRAM memory cell connected to a bit line, and forming a portion of a memory array.

Figs. 5 and 6 illustrate an alternative embodiment of the present invention. Referring initially to Fig. 5, wafer fragment 10 is illustrated at a processing step subsequent to that of Fig. 2, and is shown comprising a metallic aluminum layer 100 formed over dielectric material 40. Metallic aluminum layer 100 can be formed utilizing methodology described above for formation of metallic aluminum layer 36 of Fig. 1.

Referring to Fig. 6, aluminum layer 100 (Fig. 5) is converted to a dielectric material 102. Such conversion can comprise methodology similar to that described above with reference to Fig. 2 for formation of dielectric material 40 from metallic aluminum layer 36. Accordingly, dielectric material 102 can comprise one or more of aluminum oxide, aluminum nitride, or aluminum oxynitride. In particular embodiments, dielectric material 40 will comprise aluminum nitride and dielectric material 102 will comprise aluminum oxide. The aluminum nitride can have a thickness of, for example, from about 10Å to about 20Å, and the aluminum oxide can have a thickness of, for example, from about 10Å to about 20Å.

A conductive material 42 (which can be identical to described with reference to Fig. 3) is formed over dielectric material 102 to define a

capacitor structure 104 comprising electrically conductive materials 34 and 42, as well as dielectric materials 40 and 102. A difference between the capacitor structure 104 of Fig. 6 and the capacitor structure 44 of Fig. 3 is that conductive material 42 is spaced from first dielectric material 40 by second dielectric material 102 in the construction of Fig. 6, whereas in the construction of Fig. 3 the conductive material 42 is on the dielectric material 40. A similarity between the capacitor constructions 44 of Fig. 3 and 104 of Fig. 6 is that both constructions can comprise a dielectric material 40 comprising aluminum, oxygen and nitrogen on a conductive material 34. Capacitor construction 104 can be incorporated into a DRAM cell utilizing processing similar to that described above with reference to Fig. 4. Dielectric materials 40 and 102 can be considered to together define a dielectric region operatively positioned between electrical nodes 34 and 42 in the capacitor construction 104 of Fig. 6.

Another embodiment of the invention is described with reference to Figs. 7 and 8. Referring initially to Fig. 7, wafer fragment 10 is shown at a processing step which is alternative to that of Fig. 1. Specifically, wafer fragment 10 is shown comprising a silicon dioxide layer 150 formed over conductive material 34 prior to formation of metallic aluminum layer 36. Silicon dioxide layer 150 can be formed by, for example, oxidation of an upper surface of a silicon-comprising material 34, or by chemical vapor deposition of silicon dioxide over

material 34. It has been found that aluminum does not react or diffuse into clean, high-quality silicon dioxide at temperatures below 500°C, and that even at 500°C, an aluminum-silicon reaction is not detected regardless of whether there is significant amounts of water vapor, and regardless of whether the exposure time is for several hours. Accordingly, it is reasonable to deposit a controlled thickness of aluminum over a controlled thickness of thermally grown silicon dioxide, and yet to avoid interaction of the two materials.

It can be desired that a thickness of oxide material 150 be carefully controlled, and such preferably comprises utilization of methodology wherein any water utilized during formation of oxide layer 150 is ultra-pure water.

Oxide layer 150 can be formed to a controlled thickness by carefully growing the oxide layer to a desired thickness. Alternatively, oxide layer 150 can be grown beyond a desired thickness, and then carefully etched back to a desired thickness. One method for etching back an oxide is to utilize an inductively coupled plasma optical emissions spectroscopy technique, which can permit detection and determination of variations in oxide thickness to within a monolayer, and possibly to within 0.2Å.

Silicon dioxide layer 150 preferably has a thickness of from greater than 0Å to less than about 15Å, and a thickness of about 10Å can be preferred.

Referring to Fig. 8, metallic aluminum layer 36 (Fig. 7) is converted to a dielectric material 152. Such conversion can comprise, for example, exposing metallic aluminum layer 36 to conditions similar to those discussed above with reference to Fig. 2 to form dielectric material layer 152 to comprise one or more of aluminum nitride, aluminum oxide, or aluminum oxynitride. In an exemplary process, dielectric layer 152 can comprise aluminum oxynitride, and can be formed to a thickness of from about 20 to 40Å, and silicon dioxide layer 150 can comprise a thickness of from about 5Å to about 15Å, with a preferred thickness being about 10Å. In other exemplary processing, dielectric material 152 can consist essentially of, or consist of aluminum nitride, and can be formed to a thickness of, for example, from about 20Å to about 40Å, and silicon dioxide 150 can be formed to a thickness of from about 5Å to about 15Å, with about 10Å being a preferred thickness.

Conductive material 42, dielectric materials 150 and 152, and conductive material 34 together define a capacitor construction 154. Capacitor construction 154 can be incorporated into a DRAM cell utilizing methodology similar to that discussed above with reference to Fig. 4. Dielectric materials 150 and 152 can be considered to together define a dielectric region operatively positioned between electrical nodes 34 and 42 in the capacitor construction 154 of Fig. 8.

Fig. 9 illustrates yet another embodiment of the present invention, and specifically illustrates that the methodology of Figs. 7 and 8 can be combined with that of Figs. 5 and 6. Fig. 9 illustrates wafer fragment 10 comprising a capacitor structure 162 which incorporates three dielectric material layers 150, 152 and 160. Dielectric material layers 150 and 152 can be formed by the processing described above with reference to Figs. 7 and 8. Dielectric material 160 can be formed by forming a metallic aluminum layer over dielectric material 152, and subsequently converting the metallic aluminum layer to a dielectric material. Such can be conducted analogously to the processing described with reference to Figs. 5 and 6 wherein a metallic aluminum layer 100 is formed over a dielectric material 40 and subsequently converted to a dielectric material 102. Accordingly, dielectric material 160 of Fig. 9 can comprise aluminum oxide, aluminum nitride or aluminum oxynitride, and in particular embodiments can consist of, or consist essentially of aluminum oxide, aluminum nitride or aluminum oxynitride. In particular methodology, dielectric material 150 can consist of silicon dioxide, dielectric material 152 can consist of aluminum nitride, and dielectric material 160 can consist of aluminum oxide. In such embodiment, silicon dioxide material 150 can have a thickness of from about 5Å to about 15Å, aluminum nitride material 152 can have a thickness of from about 5Å to about 15Å, and aluminum oxide material 160 can have a thickness of from about 5Å to about 15Å, with exemplary thicknesses of materials

150, 152 and 160 being about 10Å each. Dielectric materials 150, 152 and 160 can be considered to together define a dielectric region operatively positioned between electrical nodes 34 and 42 in the capacitor construction 162 of Fig. 9.

The capacitor structure 162 of Fig. 9 can be incorporated into a DRAM cell utilizing methodology similar to that discussed above with reference to Fig. 4.

Fig. 10 illustrates yet another embodiment of the present invention, and shows wafer fragment 10 at a processing step subsequent to that of Fig. 1. Specifically, a metallic aluminum layer 36 of Fig. 1 has been transformed to a dielectric material 170 analogously to the formation of dielectric material 40 of Fig. 2. However, in contrast to the processing described above with reference to Fig. 2, the formation of dielectric material 170 has caused formation of a silicon dioxide layer 172 under dielectric material 170. Such can occur if dielectric material 170 comprises aluminum oxide or aluminum oxynitride, and if oxygen utilized during the transformation of metallic aluminum layer 36 (Fig. 1) to dielectric material 170 permeates the aluminum layer to interact with a silicon-comprising material 34 and oxidize an upper portion of the material. Such can occur if, for example, an aluminum oxide or aluminum oxynitride layer 170 is formed utilizing an implant of oxygen into metallic aluminum layer 36. In particular processing, silicon dioxide layer 172 will have a thickness of greater than 5Å, and can, for example,

have a thickness of about 10Å. Also, dielectric material 170 can be formed to a thickness of, for example, from about 10Å to about 40Å, with an exemplary thickness being from about 10Å to about 20Å.

Referring to Fig. 11, subsequent processing can be utilized to form a conductive material 42 over dielectric material 170, and accordingly to define a capacitor construction 174 comprising conductive material 42, dielectric materials 170 and 172, and conductive material 34. Capacitor construction 174 can be incorporated into a DRAM cell utilizing methodology similar to that discussed above with reference to Fig. 4.

In compliance with the statute, the invention has been described in language more or less specific as to structural and methodical features. It is to be understood, however, that the invention is not limited to the specific features shown and described, since the means herein disclosed comprise preferred forms of putting the invention into effect. The invention is, therefore, claimed in any of its forms or modifications within the proper scope of the appended claims appropriately interpreted in accordance with the doctrine of equivalents.